# REMARKS

## A. SUMMARY OF THE AMENDMENTS

The present application still contains 44 claims numbered 1 to 44.

Four paragraphs of the specification have been amended as described above in the Section entitled "AMENDMENTS TO THE SPECIFICATION".

Figs. 1, 5, 9, 14, 17A and 20 have been amended as described above in the Section entitled "AMENDMENTS TO THE DRAWINGS".

No new subject matter has been added by way of the present amendment.

## B. OBJECTION TO THE DRAWINGS

On page 2 of the Office Action, the Examiner has objected to the drawings for failing to comply with 37 CFR 1.84(p)(5).

Fig. 4

The Examiner has referred to various passages on pages 40-43 where reference is made to "queue controllers $710_1$, $710_2$, $710_3$, $710_4$". However, it is noted that this description accompanies Fig. 7 and not Fig. 4. Thus, the Applicant suspects that the Examiner intended to object to Fig. 7 rather than to Fig. 4.

In response, rather than amend Fig. 7, the Applicant has elected to amend the specification. Specifically, the specification now states more clearly that transmitter 140 comprises N queue controllers $710_j$, $1 \leq j \leq N$, and it is

specified that N can be any positive integer including 4. Therefore, it is respectfully submitted that all reference signs referred to in the description of Fig. 7, and in particular "queue controllers $710_1$, $710_2$, $710_3$, $710_4$", are present in Fig. 7, either expressly or impliedly, and it is respectfully submitted that Fig. 7 is in full compliance with 37 CFR 1.84(p)(5).

Fig. 5

The Examiner has objected to Fig. 5 for failing to include the reference signs corresponding to "slots $508_A$, $508_B$, $508_C$" and "entries $514_A$, $514_B$, $514_C$". In response, the Applicant has amended Fig. 5 and respectfully submits that Fig. 5 is in full compliance with 37 CFR 1.84(p)(5).

Fig. 9

The Examiner has objected to Fig. 9 for failing to include the reference signs corresponding to "transmitter 940" and "base_address line 982". In response, the Applicant has amended Fig. 9 and respectfully submits that Fig. 9 is in full compliance with 37 CFR 1.84(p)(5).

Fig. 11

The Examiner has objected to Fig. 11 for failing to include the reference signs corresponding to "interconnect pattern 112". The Applicant traverses this rejection. It is respectfully submitted that the portion of the description which concentrates on Fig. 11 is not isolated with respect to the other Figures in the application. In this case, Fig. 1 provides the requisite reference sign 112 that is referred to in the portion of the description that concentrates on Fig. 11.

Fig. 20

The Examiner has objected to Fig. 20 for failing to include the reference signs corresponding to "free_slot lines 207". In response, the Applicant has

amended Fig. 20 and respectfully submits that Fig. 20 is in full compliance with 37 CFR 1.84(p)(5).

Fig. 14

The Examiner has objected to Fig. 14 for failing to include the reference signs corresponding to "bus 1472". In response, the Applicant has amended Fig. 14 and respectfully submits that Fig. 14 is in full compliance with 37 CFR 1.84(p)(5).

Fig. 16

The Examiner has objected to Fig. 16 for failing to include the reference signs corresponding to "transmitter 1440". The Applicant traverses this rejection. It is respectfully submitted that the portion of the description which concentrates on Fig. 16 is not isolated with respect to the other Figures in the application. In this case, Fig. 14 provides the requisite reference sign 1440 that is referred to in the portion of the description that concentrates on Fig. 16.

Fig. 1

The Examiner has objected to Fig. 1 for using reference numbers " 116' " and " 116'' " containing inverted commas. In response, the Applicant has amended Fig. 1 and the accompanying portion of the description such that "traces 116'' " and "releasable connector 116' " have been replaced by "traces 117" and "releasable connector 119", respectively.

## C. REJECTION OF CLAIM 10 UNDER 35 U.S.C. 112

On page 5 of the Office Action, the Examiner has rejected claim 10 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner has requested more clarification on

page 14, lines 31-32 as to the concept and exact meaning (as well as the visual diagram) of "other patterns such as a hypercube or three- (or higher-) dimensional toroidal mesh can similarly be created using the cells...".

With respect, the Applicant submits that the interconnectivity of hypercube switch fabrics and toroidal mesh switch fabrics has been well studied for many years. For example, the CONNECTIONS MACHINE CM-1 supercomputer from Thinking Machines Corporation used a 16-dimensional hypercube fabric (*circa* mid-1980s), while Intel Corporation's PARAGON series of supercomputers used a toroidal mesh fabric (*circa* early 1990s). In order to assist the Examiner in visualising the various structures, the Applicant has performed a background search and has located the following example URL:

http://www.cs.wisc.edu/~tvrdik/5/html/Section5.html#AAAAAMesh-based%20topologies.

Should the Examiner maintain the rejection of claim 10, the Examiner is respectfully requested to provide further reasoning as to why such rejection would be maintained in light of the information provided herein.

## D. REJECTION OF CLAIMS 1-8 AND 12[*sic*]-44 UNDER 35 U.S.C. 102

On page 5 of the Office Action, the Examiner has rejected claims 1-8 and 12[*sic*]-44 under 35 U.S.C. 102(e) as being anticipated by Chang *et al.* U.S. Patent 6,731,631 (hereinafter referred to as Chang). It is noted on page 9 of the Office Action that the Examiner has also rejected claim 11 under the same grounds. The Applicant respectfully traverses this rejection and submits that claims 1-8 and 11-44 are in allowable form, as set forth herein below.

Claim 1

The Examiner's attention is directed to the following limitation of claim 1:

> "a control entity to control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell."

The Examiner contends that Chang discloses the above-identified limitation. To support his contention, the Examiner refers to Chang's port controllers 202a,b,c,d and 302a,b of Figs. 2 and 3, respectively, as well as col. 9, lines 20-25 of Chang.

However, none of these passages deals with "releas[ing] data packets [...] on a basis of a degree of occupancy of the memory in [the] destination cell." The free cell manager 416 referred to by Chang in col. 9, lines 20-25 simply "manages the external packet buffer space and notifies the Ingress DMA 404 of available space in memory for storing data and frees up memory space after data (i.e., processed packets) is retrieved by the output oriented scheduler 412".

Specifically, if the given port controller on which Chang's free cell manager 416 is located is ***not*** the destination cell, then it is clear that the free cell manager 416 does ***not*** itself control the release of packets to other port controllers, as such transmission is entirely at the mercy of the output oriented scheduler 412. On the other hand, if the given port controller 416 on which Chang's free cell manager 416 ***is*** the destination cell, then it is clear that the free cell manager 416 only affects operation of the ingress DMA 410, which is on the ***same*** given port controller, and thus does ***not*** result in control of transmission of packets to itself (i.e., to the given port controller).

In short, at least one limitation of claim 1 is not taught or suggested in Chang and therefore a rejection under 35 U.S.C. 102 is improper. The Examiner is therefore respectfully requested to withdraw his rejection of claim 1.

(*In addition, and notwithstanding the above, the Applicant respectfully draws the Examiner's attention to Chang's column 5, line 33, where the term used is*

*"chipset", which connotes a set of chips, and not the singular "chip". The Applicant also respectfully draws the examiner's attention to Chang's description of Figure 4 in col. 7 and 8, and specifically to col. 8, lines 3-4. This passage shows that the memory managed by the DRAM controller and the free cell manager described in column 9 lines 20-25 is an external memory (i.e., is located on another chip). For this additional reason, the Examiner is respectfully requested to withdraw his rejection of claim 1.*)

Claims 2-8 and 11-44

These claims are all either directly or indirectly dependent on claim 1 and therefore include all the limitations of claim 1, including those already shown to be absent from Chang. Thus, for the same reasons as those set forth above in support of claim 1, the Examiner is requested to withdraw the rejection of claims 2-8 and 11-44.

## E. REJECTION OF CLAIMS 9-10 UNDER 35 U.S.C. 103

On page 18 of the Office Action, the Examiner has rejected claims 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Chang *et al.* U.S. Patent 6,731,631 (hereinafter referred to as Chang) in view of McCrosky et al. U.S. Patent 6,741,552 (hereinafter referred to as McCrosky). The applicant respectfully traverses this rejection and submits that claims 9 and 10 are in allowable form, as set forth herein below.

Firstly, claims 9 and 10 are all both dependent on claim 1 and therefore include all the limitations of claim 1, including those already shown to be absent from Chang. Specifically, it has been shown that Chang fails to teach or suggest:

"a control entity to control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell."

Moreover, it is respectfully submitted that the above limitations are also absent from McCrosky, which is directed to a cell switching architecture based on a network of switching elements connected in the manner of a hypercube to form a switch fabric. Specifically, McCrosky lacks any description of memory occupancy or, more specifically, of controlling the release of data packets on a basis of a degree of occupancy of the memory in the destination cell.

In view of the foregoing, it is clear that there is at least one limitation of claims 9 and 10, which is not taught or suggested in the cited art. It follows that at least one of the criteria required for establishing a *prima facie* case of obviousness in accordance with MPEP 706.02(j)[1] has not been satisfied. The Examiner is therefore respectfully requested to withdraw the rejection of claims 9-10, which are believed to be in condition for allowance.

[1] For the Examiner to establish a *prima facie* case of obviousness, three criteria must be considered: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all of the claim limitations. MPEP §§ 706.02(j), 2142 (8th ed.).

## CONCLUSION

In view of the foregoing, Applicant is of the view that claims 1-44 are in allowable form. Favourable reconsideration is requested. Early allowance of the Application is earnestly solicited.

If the application is not considered to be in full condition for allowance, for any reason, the Applicant respectfully requests the constructive assistance and suggestions of the Examiner in drafting one or more acceptable claims pursuant to MPEP 707.07(j) or in making constructive suggestions pursuant to MPEP 706.03 so that the application can be placed in allowable condition as soon as possible and without the need for further proceedings.

Respectfully submitted,

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